

## Part III

### Chapter 9

# Pulse Referenced Control

Recall from Chapter 3, that naturally sampled PWM provides optimal modulator performance from a theoretical perspective. It was furthermore shown that there are significant complications in the implementation of digital PCM-PWM conversion. Nevertheless, the digital PMA topology is appealing from a theoretical point of view, in applications where the source material is digital. No analog modulator or carrier generator is needed and the digital modulator can provide a very consistent good performance. As clarified in chapter 4, the non-linearity of the switching power stage presents a significant impediment to maintain the modulator performance throughout the subsequent power conversion by a switching power stage. Unfortunately, no methods have been presented for power amplification of an already pulse-modulated signal, which incorporates effective means to compensate or eliminate these error sources. The extensive research activity within digital PMA systems has almost exclusively focused on the digital signal processing aspects.

This chapter investigates solutions to this fundamental problem that has persisted in digital PMA systems. A novel pulse referenced control method is proposed – henceforth referenced to as *Pulse Edge Delay Error Correction (PEDEC)*<sup>1</sup>. The PEDEC concept is introduced as a general method for enhanced power amplification of a pulse modulated

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<sup>1</sup> PEDEC topologies and design methods are protected by a pending patent under the PCT agreement (PCT/DK98/00133). The rights of the author and co-applicant (Bang&Olufsen A/S) shall be respected.

signal. Following, the method is applied to digital PMA systems, and three general digital PMA topologies are proposed.

## 9.1 Fundamental considerations

Undoubtedly, a switching power amplification stage can be tuned to high linearity, much better performance than that of linear output stages. However, this is a complex task that requires e.g. (see Chapter 4):

- Perfect control over the switching transitions.
- Power supply stabilization., i.e. a low noise switch mode supply is needed.
- A linear filter. The filter design gets more complicated, and requires much attention. Linear core-materials are necessary.

Obviously, direct digital PCM-PWM based power conversion will never be very *elegant* or *practical*. A control system is desirable to eliminate this dependency of the many uncontrollable parameters relating to semiconductor physics, magnetics etc, such that the performance is controlled by a few e.g. passive components. The control system should be able to correct *effectively* for power stage errors by *simple* means. This will lead to improved and much more consistent performance than can be achieved with any power output stage operating open loop.

Digital PMAs do not have an analog reference to enable linear control systems as e.g. MECC to be applied. Digital feedback control referenced to the digital source, as shown in Fig. 9.1, requires an A/D converter (or more in case of a multiple sourced control system as MECC), which renders this straightforward approach both impractical and non-elegant. The inevitable errors and failings of the A/D converter are not compensated for due the placement of the converter in the feedback path. Nothing would be gained if the saving the demodulation filter from the D/A converter [Ni96] requires the introduction of a complex, precision A/D converter. Digital feedback control for digital PMAs has been investigated [Sm94] in terms of a ripple-shaping algorithm to compensate power supply perturbations. Unfortunately, besides requiring A/D conversion this leaves all other error sources in the switching power amplification stage unchanged. An interesting alternative approach to power stage error correction was presented in [Lo94], using a quantized pulse edge correction based on an analog delay line. Unfortunately, the correction effect was shown to be difficult to predict, and the correction system has its own error sources, e.g. noise generated from the quantized pulse length correction. For practical digital PMA realization, a method for improved power amplification of an already pulse modulated signal is required, where all error sources related to the power stage and demodulation filter are effectively suppressed. A novel pulse referenced control method is presented in the following, in an attempt to realize this primary objective.

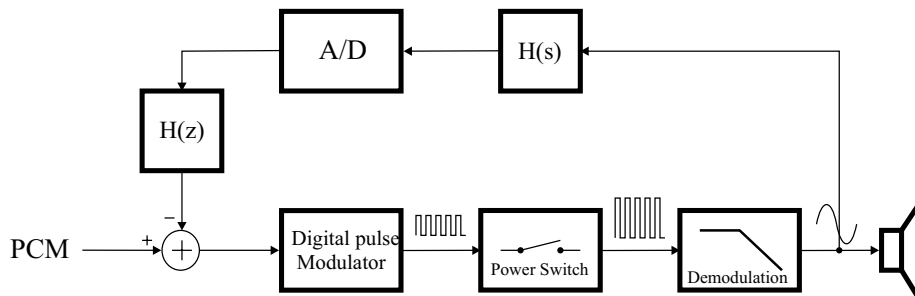


Fig. 9.1 Digital PMA based on digital feedback.

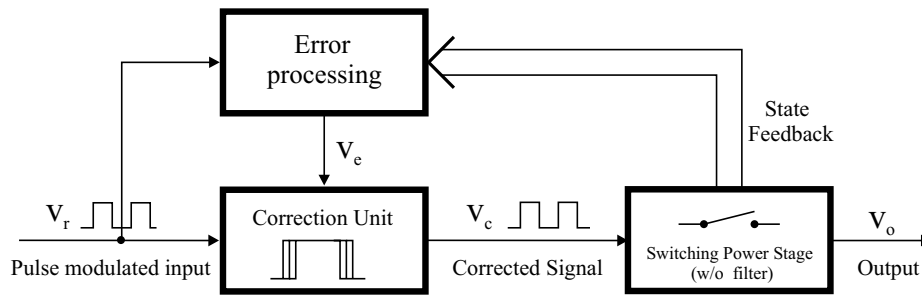


Fig. 9.2 Basic principle of Pulse Edge Delay Error Correction (PEDEC).

## 9.2 Pulse Edge Delay Error Correction (PEDEC)

Pulse Edge Delay Error Correction (PEDEC) [Ni97c], [Ni98b] is a novel general pulse referenced control method for enhanced power amplification of a pulse modulated signal. Applications are digital PMAs and general DC-DC and DC-AC power amplification where accurate and distortion free power amplification of a pulse-modulated signal is required. The basic idea is to introduce a correction unit in-between the (ideal) pulse modulator and the switching power amplification stage. The general block diagram for a PEDEC controller is shown in Fig. 9.2. The modulator output is feed to a correction unit that provides compensation by intelligently delaying the individual pulse edges, controlled by an input control signal. The re-timing is controlled to have a “pre-distorting” effect, such that the resulting switching power stage output is free from distortion, noise or any other undesired contribution. The validity of this approach are two fundamental facts:

- Digital modulators will generate a high quality output. The pulse-modulated signal may as such be used as reference for error correction.
- *All* power stage error sources can be corrected by intelligent pulse re-timing, *and* all error sources only need minor pulse edge re-timing for perfect elimination.

A perfect reproduction of the modulated signal requires that the pulse-to-pulse integrated average within each cycle (or within a few cycles) be maintained. A drop in power supply level can easily be compensated for by a widening of the pulse within the cycle interval, since the output is obtained by averaging (i.e. low-pass filtering) of the pulse modulated signal. The general structure of a PEDEC controller is shown in Fig. 9.3. The general controller can be viewed as a dual reference input pulse reference feedback control system comprising:

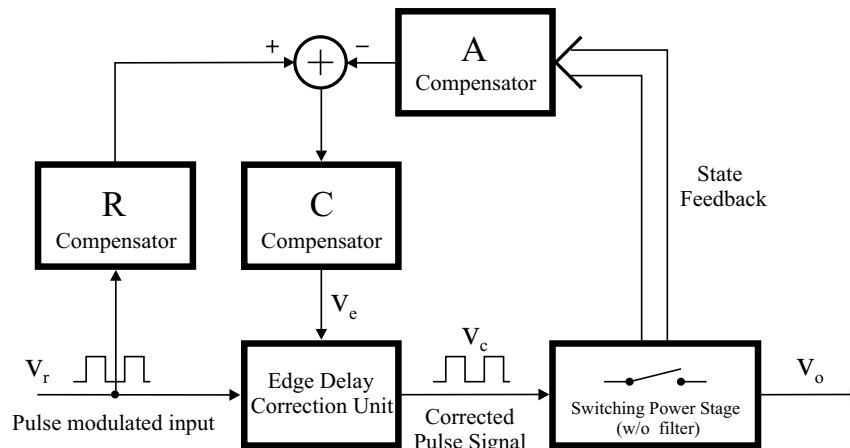


Fig. 9.3 The general elements of a PEDEC controller.

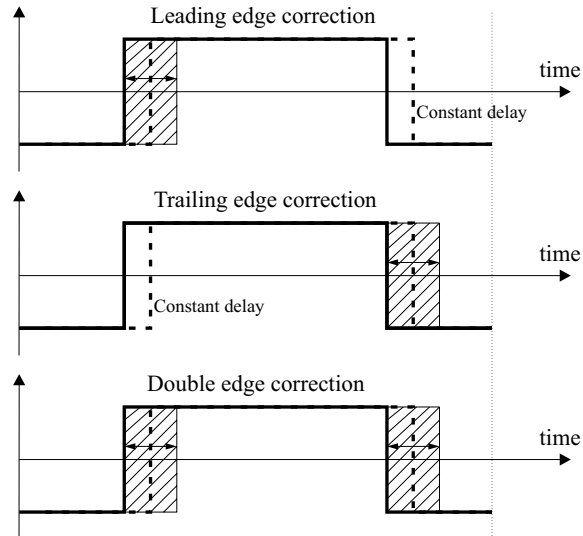


Fig. 9.4 Basic approaches to PEDEC implementation.

- The PEDEC unit with means to control the delays of the individual edges on the reference input  $v_r$ , based on a control input  $v_e$ . The PEDEC unit output is the corrected or “pre-distorted” signal.
- A state feedback block  $A$  that includes compensation from the power stage block.
- An optional reference shaping block  $R$  that serves to optimize the error estimation.
- A subtraction unit to generate error information.
- A compensator  $C$  to shape the error that feeds the PEDEC unit ( $v_e$ ).

Several approaches to pulse edge correction are illustrated conceptually in Fig. 9.4. Both leading edge, trailing edge or double edge delay error correction are feasible solutions. The following sections will introduce a range of new parameters, defined in Table 9.1, in order to provide a coherent analysis.

### 9.2.1 Control function specification

A central aspect is the specification of the PEDEC unit control function. For simple analysis and implementation, it is of course desirable with the simplest possible control function. Let the control error signal to the PEDEC unit realize a controlled function on the pulse edges, such that the effective change in pulse width  $\Delta t_w$  at the end of the switching cycle is proportional to the control signal  $v_e$ :

$$\Delta t_w = k_w \cdot v_e \quad (9.1)$$

I.e:

$$\frac{dt_w}{dv_e} = k_w \quad (9.2)$$

Parameter	Description
$v_e$	Control error signal to PEDEC unit
$v_r$ ( $\tilde{v}_r$ )	Reference signal (pulse modulator output). ( $\sim$ ) indicates the average or low frequency part of the signal.
$v_c$ ( $\tilde{v}_c$ )	Pulse edge delayed PEDEC unit output voltage. ( $\sim$ ) indicates the average or low-frequency component of the modulated signal.
$t_s$	Switching period.
$t_0$	Central PEDEC unit parameter, corresponding to the maximal effective pulse width change.
$t_l, \hat{t}_l$	Leading edge transition time before and after ( $\wedge$ ) correction
$t_t, \hat{t}_t$	Leading edge transition time before and after ( $\wedge$ ) correction
$t_w, \hat{t}_w$	Pulse width before and after ( $\wedge$ ) correction: $t_w = t_t - t_l$
$V_R$	Pulse modulator output voltage level.
$V_I$	Limited integrator output pulse voltage level.
$V_C$	PEDEC unit output pulse level.
$V_{CC}$	Power rail voltage level.

Table 9.1 Definition of fundamental PEDEC parameters.

By averaging within a single switching cycle, the relationship between an increment in pulse width  $\Delta t_w$  and the corresponding change in the average of the PEDEC output  $\Delta \tilde{v}_c$  can be established. Assuming for simplicity here, that the PEDEC output pulse amplitude is unity:

$$\Delta \tilde{v}_c = \frac{1}{t_s} \left( \int_0^{d \cdot t_s + \Delta t_w} 1 \cdot dt + \int_{d \cdot t_s + \Delta t_w}^{t_s} (-1) \cdot dt \right) = \frac{2}{t_s} \Delta t_w \quad (9.3)$$

Where  $d$  is the duty-cycle within the present switching cycle. Hence:

$$\frac{d\tilde{v}_c}{dt_w} = \frac{2}{t_s} \quad (9.4)$$

Combining (9.2) and (9.4), the fundamental linear PEDEC control function arrives:

$$k_{PEDEC} = \frac{d\tilde{v}_c}{dv_e} = \frac{2k_w}{t_s} \quad (9.5)$$

Such a simple linear control function dramatically simplifies PEDEC controller design, since the whole machinery of linear control system design and verification can be fully utilized. Obviously, other control functions (e.g. non-linear functions) could be interesting alternatives for PEDEC. This could be a subject for future research.

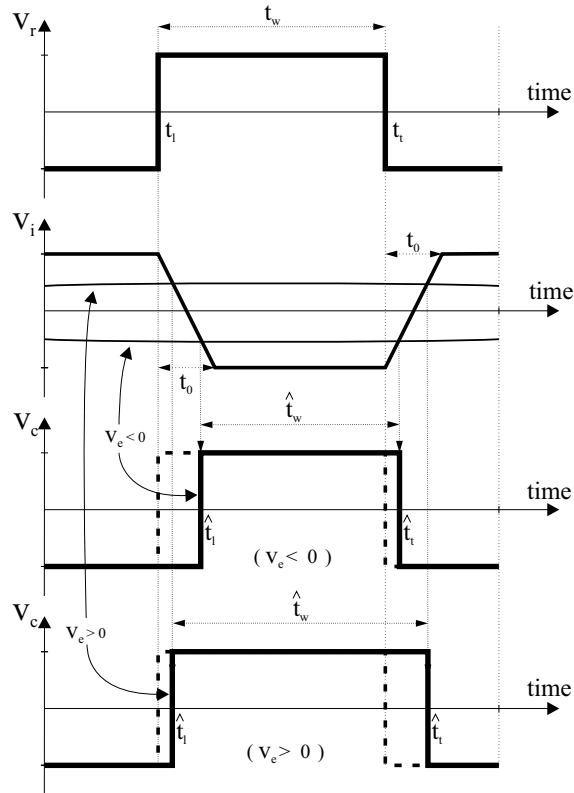


Fig. 9.5 Proposed realization of a linear double edge PEDEC control function.

## 9.2.2 Realizing the control function

This section proposes a simple approach to implement the double sided PEDEC unit, which implements the above specified control function. The method is shown in Fig. 9.5. The pulse delay correction is realized by a limited integration of the incoming (ideal) pulse waveform generating the signal  $v_i$ , and comparing this modified reference with the control signal  $v_e$ . The effective pulse width change,  $\Delta t_w$ , will be the difference between the leading edge delay and the trailing edge delay. From Fig. 9.5 it is obvious that  $v_e > 0$  will increase the pulse width, whereas  $v_e < 0$  will lead to a negative  $\Delta t_w$ . The following relations are obtained from the proposed double edge correction scheme in Fig. 9.5:

$$\hat{t}_l = t_l + \frac{t_0}{2} + t_0 \frac{v_e}{2V_I}, \quad \hat{t}_t = t_t + \frac{t_0}{2} - t_0 \frac{v_e}{2V_I} \quad (9.6)$$

$\Delta t_w$  is derived:

$$\hat{t}_w = \hat{t}_t - \hat{t}_l = t_w - t_0 \frac{v_e}{V_I} \Rightarrow \Delta t_w = \hat{t}_t - \hat{t}_l = \begin{cases} t_0 & (v_e > V_I) \\ t_0 \frac{v_e}{V_I} & (-V_I \leq v_e \leq V_I) \\ -t_0 & (v_e < -V_I) \end{cases} \quad (9.7)$$

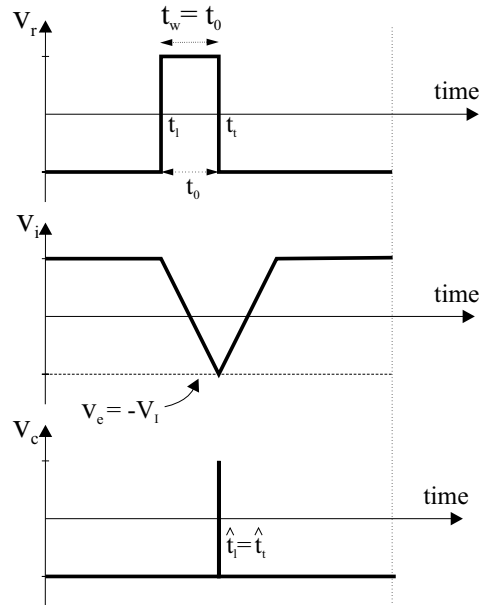


Fig. 9.6 PEDEC constraints on minimal pulse width.

In other words  $k_w$  as defined in (9.1) is:

$$k_w = \frac{dt_w}{dv_e} = \frac{t_0}{V_I} \quad (9.8)$$

From Fig. 9.5, the following relationship between an increment in pulse width  $dt_w$  and  $\tilde{v}_c$  is established:

$$\frac{d\tilde{v}_c}{dt_w} = \frac{2V_C}{t_s} \quad (9.9)$$

Combining (9.8) and (9.9):

$$k_{PEDEC} = \frac{d\tilde{v}_c}{dv_e} = \frac{2V_C}{V_I} \frac{t_0}{t_s} \quad (9.10)$$

Assuming without loss of generality that the pulse amplitudes are adjusted to  $V_C = V_I$ , the following expression of the equivalent PEDEC unit control gain emerge:

$$\boxed{k_{PEDEC} = \frac{2t_0}{t_s}} \quad (9.11)$$

The validity of this simple linear model will be investigated throughout the simulation and verification of various topologies later in this chapter.

For optimal control with the proposed PEDEC block realization, the pulses need to have a certain minimal width. This limits the available modulation index range with digital PWM. The *minimum* pulse width is related to the modulation index  $M$  and switching period  $t_s$  as:

$$t_{w,\min} = (1-M) \frac{t_s}{2} \quad (9.12)$$

Since the minimal pulse width for correct PEDEC operation is indeed  $t_0$  as illustrated in Fig. 9.6 the maximum modulation index is:

$$t_{w,\min} \geq t_0 \Rightarrow M_{\max} = 1 - \frac{2t_0}{t_s} \quad (9.13)$$

This constraint on pulse width and modulation index does not present a fundamental limitation, since the correction will still work partially beyond this limit. The situation in Fig. 9.6 is the absolute worst case, where the control voltage takes its *maximal* negative value. The digital input signal to the PMA could be limited at  $M_{\max}$  for optimal control performance within the complete operating range for the PMA. Such a limitation is straightforward to implement in the digital domain.

### 9.3 Applying PEDEC to Digital PMA systems

PEDEC can be considered as a general control method for improved power amplification of a pulse-modulated signal. The generality of the principle means that it can be used advantageously in combination with a range of different control structures. With the linear control function within the PEDEC unit, a linear model for PEDEC based digital PMA can be derived. Following, the controller design may follow the general 6-step methodology for controller design and verification. However, there are some significant differences between linear controller design for analog PMAs, and linear controller design using PEDEC. First of all, the loop in the PEDEC based system does not enclose a modulator. The equivalent linear gain of the power is the pulse amplification factor:

$$K_P = \frac{V_{CC}}{V_R} \quad (9.14)$$

Another significant difference is the effects of  $v_p$ , i.e. the tradeoffs between bandwidth and carrier frequency is different. An interesting property of PEDEC control is that the noise from  $v_p$  may be nearly eliminated by proper reference shaping (R), such that the noise on the control signal  $v_e$  is also minimized. PEDEC also differs from conventional control systems by the limited correction range of the PEDEC unit. This has significant importance in terms of gain control in that the range of system gain adjustment will be limited. Furthermore, the switching frequency has determining influence on the control system. This has to be taken into account during controller design.

#### 9.3.1 Defining control structures

Three basic topologies based on single loop control are defined and investigated in more detail in the following. The topologies differ mainly in terms of feedback source and error estimation. The double edge PEDEC unit will be used throughout the investigations.

Without loss of generality, it is assumed throughout the investigations, that the pulse levels in the controller are identical, i.e.  $V_R = V_C = V_I$ . The three topologies are introduced below.

### PEDEC Voltage Feedback Control – Type 1 (VFC1)

PEDEC VFC1 is characterized by a voltage feedback from the switching power stage output  $v_p$ . The feedback path compensator is a simple attenuation, and the compensator block  $C$  is a linear filter. The topology is furthermore characterized by a *zero order reference shaping*, i.e. the reference shaping block  $R$  is completely omitted such that the error estimation is based on a direct comparison of input and output pulses. Despite the simple controller structure of PEDEC VFC1, the system introduces a powerful and flexible control of system performance.

### PEDEC Voltage Feedback Control – type 2 (VFC2)

PEDEC VFC2 resembles PEDEC VFC1 in terms of feedback source. However, the topology differs by *first order reference shaping* in combination with a *matched first order output feedback shaping* in the  $A$  block. This also led to different compensator characteristics ( $C$ ).

### PEDEC Voltage Feedback Control – type 2 (VFC3)

PEDEC VFC3 differs significantly from the other two topologies by utilizing *global* feedback from  $v_o$ , in combination with *second order reference shaping* for optimal error estimation. Including the filter in the loop significantly changes the compensator characteristics.

The three topologies will be subjected to a detailed investigation in the following. Loop shaping methods will be addressed by presenting a general frequency normalized loop synthesis methods. Following, illustrative case example will be synthesized and evaluated for each topology.

## 9.4 PEDEC VFC1

The control structure is shown in Fig. 9.7. Despite the simplicity of the controller, the system enables powerful control of the performance of the switching power amplification stage. Note how the audio signal remains digital or pulse modulated throughout the main audio chain. No analog modulator or carrier generator is needed in the digital PMA system. The system is essentially controlled by the digital modulator.

### 9.4.1 Analysis

Given the linear control function in (9.11), it is straightforward to derive the equivalent linear model of the system as shown in

Fig. 9.8. The individual elements of the controller are also defined in the figure. The loop components are:

$$\begin{cases} C(s) = K_C \frac{(\tau_{z1}s + 1)}{(\tau_{p1}s + 1)(\tau_{p2}s + 1)(\tau_{p3}s + 1)} \\ B(s) = K_P k_{PEDEC} \\ A(s) = \frac{1}{K} \\ R(s) = 1 \end{cases} \quad (9.15)$$

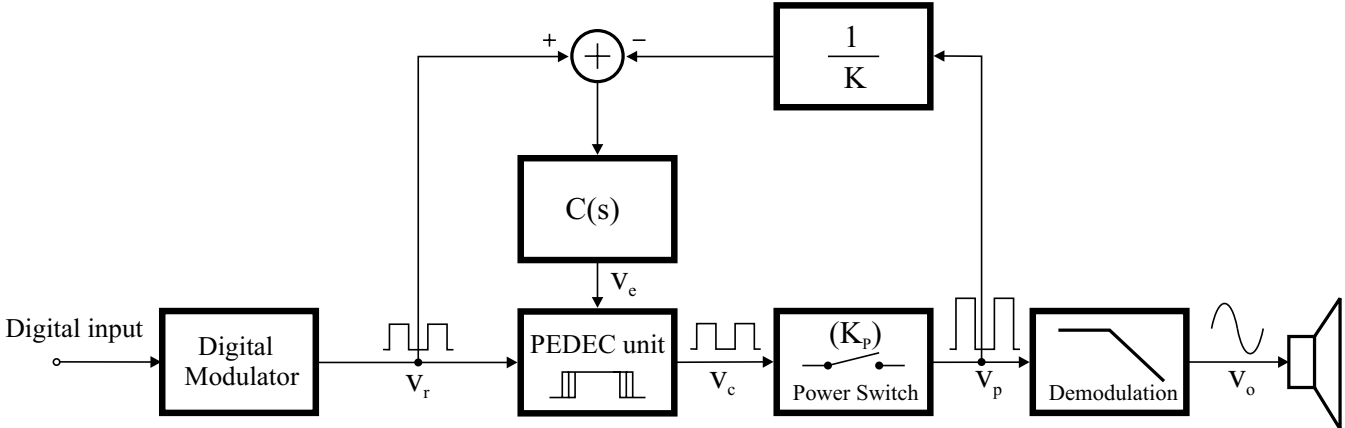


Fig. 9.7 PEDEC VFC1 Topology.

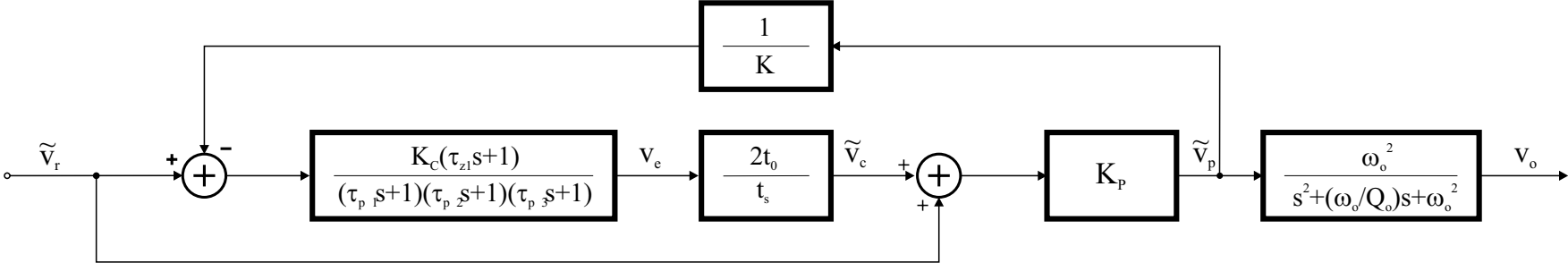


Fig. 9.8 Dual input linear model of PEDEC VFC1 Topology with all compensator elements defined.

The C compensator provides sufficient flexibility for loop optimization. The loop transfer function is:

$$L_1(s) = \frac{K_P k_{PEDEC} K_C}{K} \frac{(\tau_{z1}s + 1)}{(\tau_{p1}s + 1)(\tau_{p2}s + 1)(\tau_{p3}s + 1)} \quad (9.16)$$

The compensator gain  $K_C$  has to be tuned to realize the desired loop bandwidth. The linear model in Fig. 9.7 illustrates the *dual* input configuration, i.e. the system transfer function from  $v_r$  to  $v_p$  has two contributions:

$$\begin{aligned} H(s) &= \frac{C(s)B(s)}{1 + A(s)C(s)B(s)} + \frac{K_P}{1 + A(s)B(s)C(s)} \\ &= \frac{K_P [C(s)k_{PEDEC} + 1]}{1 + A(s)C(s)B(s)} \end{aligned} \quad (9.17)$$

In the special but not unusual case where  $K = K_P$ , the transfer function is *constant*:

$$H(s) = \frac{K [C(s)k_{PEDEC} + 1]}{1 + C(s)k_{PEDEC}} = K \quad (9.18)$$

This characteristic is significantly different from the previously analyzed control methods. The explanation is that PEDEC VFC1 is *only contributing to system performance as all as long as there are errors present*. In the general case, corresponding to  $K \neq K_P$ :

$$H(s) \approx \begin{cases} K & (f < f_u) \\ K_P & (f \gg f_u) \end{cases} \quad (9.19)$$

$K \neq K_P$  can be viewed as a linear error that the PEDEC controller will attempt to correct for. Obviously, this correction is only possible within the bandwidth of the system. With a standard second order filter for demodulation:

$$F(s) = \frac{\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \quad (9.20)$$

The system transfer function will essentially be determined by the demodulation filter.

### 9.4.2 PEDEC VFC1 loop shaping

Table 9.2 proposed a set of general system parameters. The specification of the PEDEC unit gain is based on an estimation of the necessary correction range, and the specified gain of 0.2 represents a good compromise. A higher  $k_{PEDEC}$  compromise the modulation index range with optimal control and the lower gain on the other hand compromises the range of error size. This will especially be a problem in terms of the correction of large magnitude linear errors.

Parameter	Value	Comment
$k_{PEDEC} = \frac{2t_o}{t_s}$	$\frac{1}{5}$	Equivalent PEDEC unit gain.
$f_{p1} = \frac{1}{\tau_{p1}}$	$\frac{1}{20}f_u$	Loop parameter
$f_{p2} = \frac{1}{\tau_{p2}}$	$f_{p1}$	Loop parameter
$f_{p3} = \frac{1}{\tau_{p3}}$	$2f_u$	Loop parameter
$f_{z1} = \frac{1}{\tau_{z1}}$	$\frac{1}{2}f_u$	Loop parameter
$f_o$	2	Filter natural frequency
$Q_o$	$\frac{1}{\sqrt{3}}$	Filter Q

Table 9.2 Proposed general parameters for PEDEC VFC1 loop shaping.

### 9.4.3 Case example

#### Specification

A case example is considered for the full audio bandwidth with a system gain of  $K = 20dB$  and an equivalent power stage gain of  $K_p = 20dB$ .

#### Synthesis

The synthesis is trivial with the defined general loop shaping procedure. The bandwidth of the considered case example is  $f_u = 5$ .

#### Verification

Fig. 9.9 shows Bode plots for each component in the loop and the resulting loop transfer function. The characteristics are much alike the VFC2 topology that was investigated in Chapter 6. The main difference is that the  $C(s)$  compensator has to have a higher gain. Fig. 9.10 shows Bode plots for the individual components that contribute the closed loop system response. The following is verified:

- Within the bandwidth of the control system, the “feed through path” is suppressed, i.e. the system is controlled exclusively by the loop.
- Around the frequency of unity gain, both paths contribute to the system response such that the system gain remains constant.
- Beyond the bandwidth of the loop, the “feed through” path exclusively determines the system response.
- With a constant gain characteristic of PEDEC VFC1, the demodulation filter determines the system response.

#### Robustness properties

PEDEC VFC1 is influenced by uncertainty on the same parameters as VFC2 in chapter 6. Since the loop transfer function characteristics are similar, the same conclusions can be drawn, i.e. PEDEC VFC1 will obey  $RS$  and  $RP$  within the  $US$ . However, it should be emphasized that the correction range of PEDEC is physically limited such that the control system will not operate correctly over the complete range of gain perturbations. The correction range is related to  $t_0$ , i.e.  $k_{PEDEC}$ .

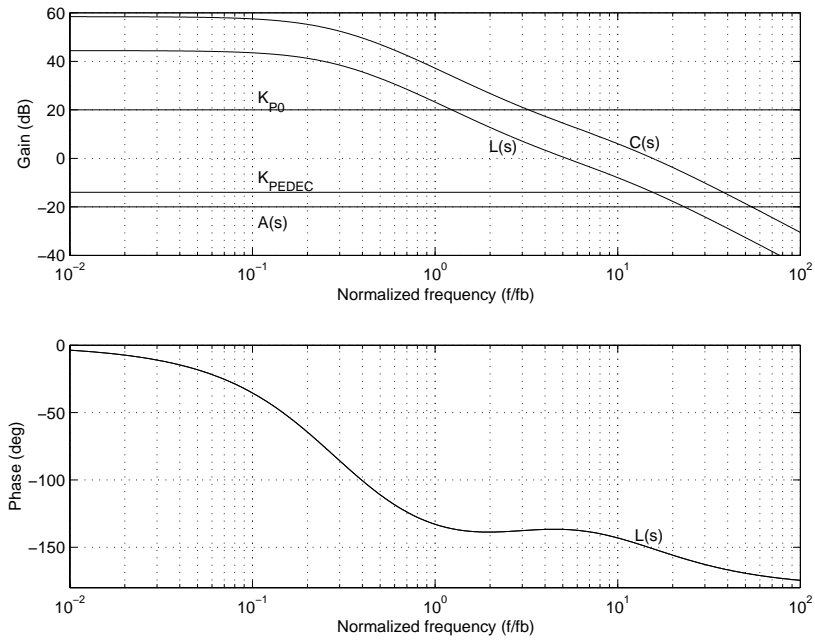


Fig. 9.9 Loop components and the resulting loop transfer function for PEDEC VFC1.

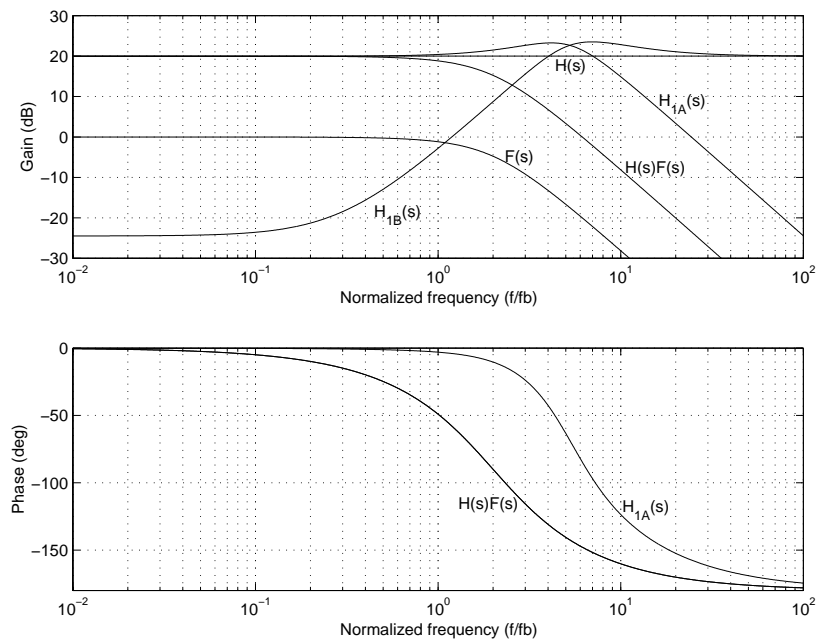


Fig. 9.10 Contributions to the system transfer function for PEDEC VFC1.

### Non-linear simulation

The system considered is again a 200W power stage, operating on a  $V_S$  power supply level. The parameters are summarized below:

Parameter	Value	Comment
$f_B$	20KHz	Bandwidth frequency
K	20dB	Amplifier gain
$V_S$	50V	Power supply rail
$f_s$	350KHz	$t_s = 2.86\mu s$
$t_0$	286ns	Realizes desired PEDEC unit gain
$V_C, V_I, V_R$	5V	Pulse amplitude levels.

There are quite a few differences between the linear feedback topologies presented in the previous chapter and a PEDEC controlled digital PMA. Some of the important differences are:

- The limited correction range.
- The dual input topology.
- The carrier frequency influences on e.g. stability.

PEDEC VFC1 has been subjected to a thorough low level simulation. The essential results will be presented in the following.

Fig. 9.11 shows a simulation of the complete PEDEC VFC1 system at idle operation. The feedback compensator output has the opposite phase of the PWM reference, such that most of the carrier related signals are eliminated at the difference point. This initial functional simulation of the system verifies that the correction system is stable and operating exactly as specified. As specified in (9.19), the system gain can be adjusted by the A-compensator in the feedback path. This is verified by the functional simulation in Fig. 9.12. The A-compensator gain is adjusted to 1/8, 1/10 and 1/12 to realize various closed loop system gains. Note the significant fundamental component in  $v_e$  where  $K \neq K_p$ . It is concluded, that the gain can be adjusted over a small range while maintaining system performance.

#### Correction of PTE

The capability to suppress PTE errors has been investigated by a parametric investigation of the near worst-case situation  $M = 0.5$ ,  $f = 5KHz$ . Fig. 9.13 shows the PEDEC unit control signal and the resulting output in the two cases  $t_d = 10ns$  and  $t_d = 100ns$ , respectively. There is no visible distortion i.e. the outputs are identical. The improvement in distortion is about 25dB, corresponding to theory. It is very interesting to observe, how the controller applies anti-distortion with by widening the pulse when the error signal with a positive error signal during the positive going cycle and vice versa. The square wave error is recognized from the distortion analysis in Chapter 4, i.e. the control signal to the PEDEC unit *directly envisions the distortion type*. A parametric analysis of THD vs.  $t_d$  is shown in Fig. 9.14. The improvement is constant and independent of  $t_d$ . Furthermore, the reduction in distortion depends on the loop gain linearly as seen from the three simulations. The frequency dependency of the correction has been verified in [Ni97c]. In general, PEDEC VFC1 provides effective control over PTE errors and the performance improvements are easily controlled.

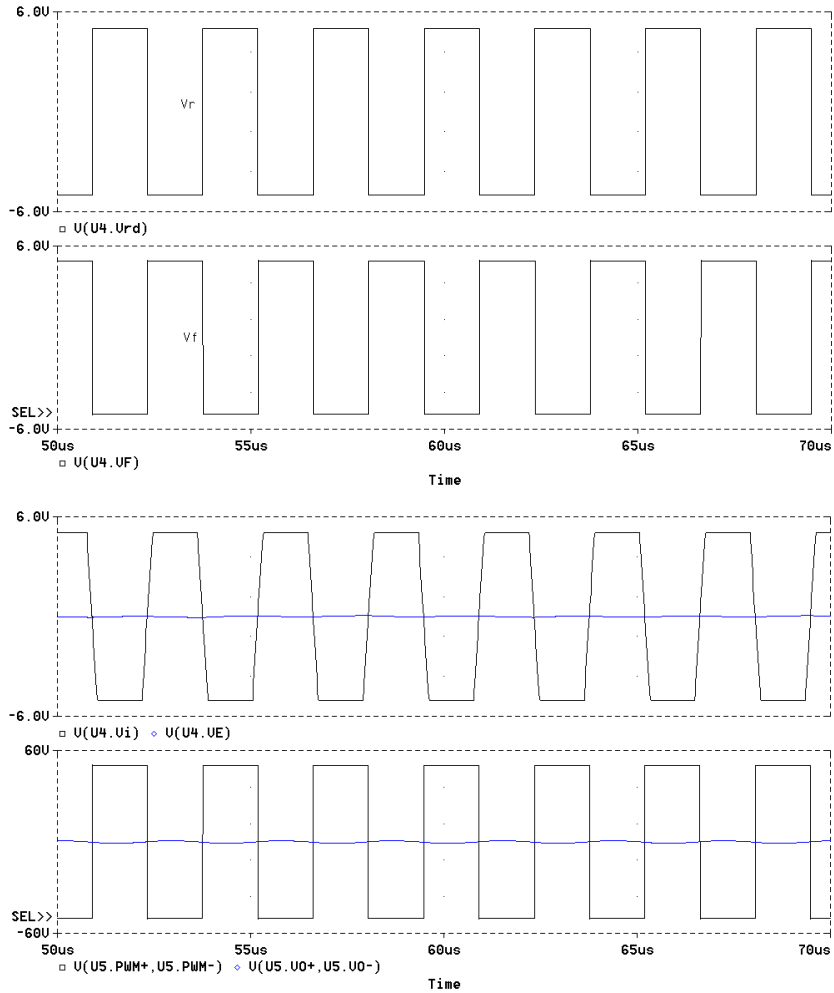


Fig. 9.11 Functional simulation of PEDEC VFC1 system. Reference input  $v_r$  and feedback  $v_f$ , PEDEC unit signals  $v_e$ ,  $v_i$  and finally the resulting corrected power stage output.

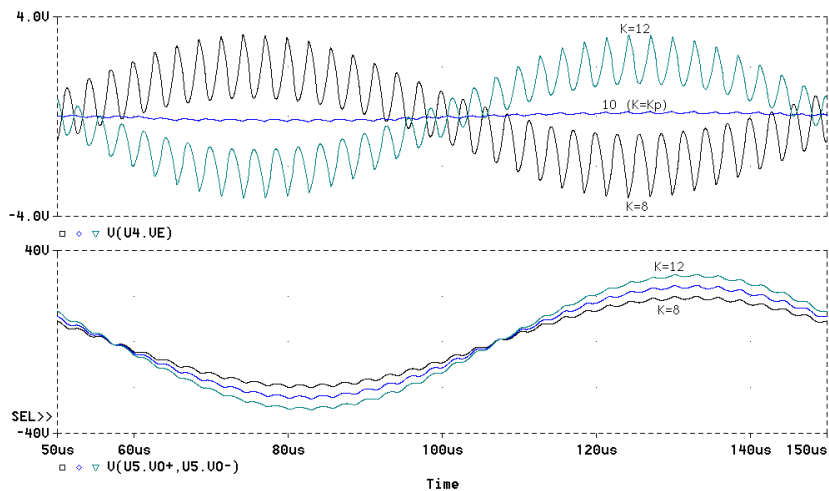


Fig. 9.12 Functional simulation of gain control with the PEDEC VFC1 Controller. A-block compensator gain is adjusted to 1/8, 1/10 and 1/12, corresponding to gains of 8, 10 and 12 respectively. Top - PEDEC unit control signal  $v_e$ . Bottom - PMA output.

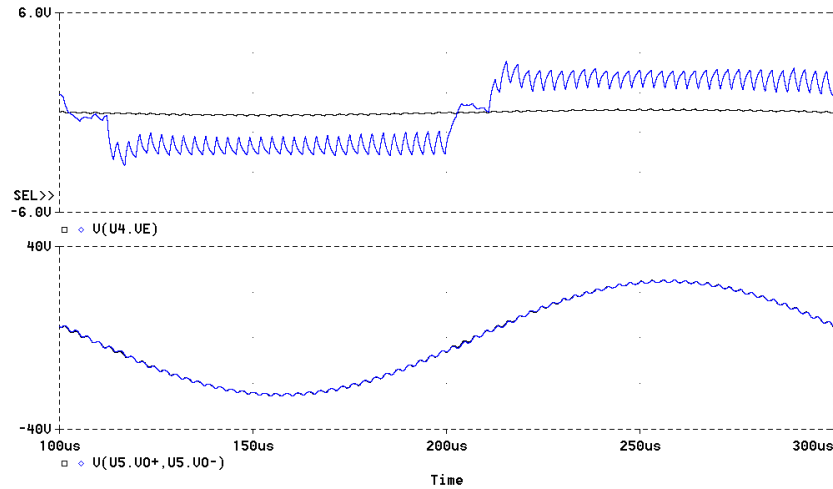


Fig. 9.13 PTE correction for PEDEC VFC1.  $M=0.5$ .  $f=5KHz$ . Top –  $v_e$  with  $t_D=10ns$  and  $t_D=100ns$ .  $v_e$  clearly envisions the distortion type. Bottom – Resulting output. Even large linear and non-linear errors are corrected effectively by the PEDEC controller.

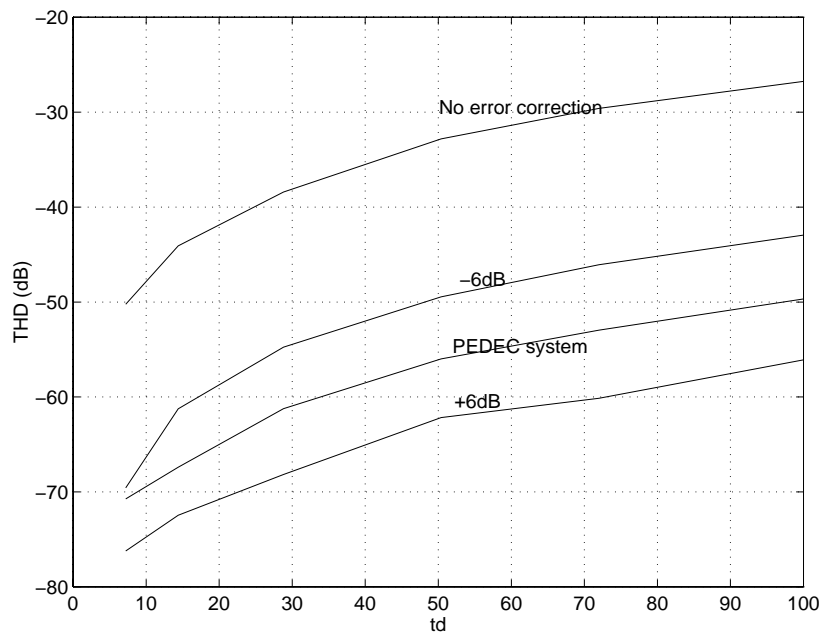


Fig. 9.14 Parametric investigation of THD vs.  $t_d$  for PEDEC VFC1. The controller improves THD 20dB - 30dB, corresponding to theory. Equally important - the performance improvements are controllable by the compensator.

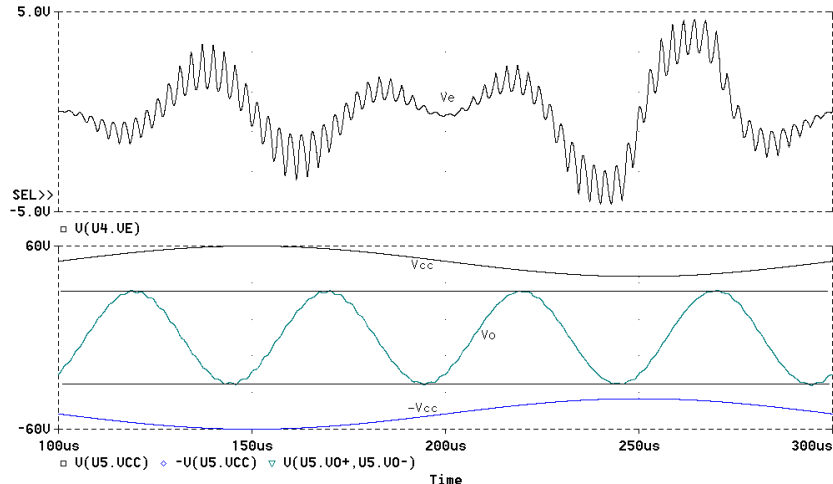


Fig. 9.15 Simulation of the correction of PAE for PEDEC VFC1. Power supply is perturbed with a 5KHZ, 10Vpp error signal.  $M=0.5$ .  $f = 20KHz$  (worst-case). The PEDEC controller effectively reduces the intermodulation and improves PSRR by about 25dB corresponding to theory.

#### *Correction of Pulse Amplitude Errors (PAE)*

Pulse amplitude errors can have significant magnitude, especially if a simple non-stabilized power supply is used. The rejection of power supply perturbations is investigated by superposing the power rail with a 5KHZ, 10Vpp harmonic perturbations. This causes an IM-distortion in the order of 5%-10% as shown in Chapter 4. Fig. 9.15 shows a simulation of the perturbed system with the PEDEC controller. The intermodulation is reduced by approximately 25dB in this worst-case situation as expected from theory, and no intermodulation is visible in the time domain. The PEDEC controller compensates for the effect by widening the pulses (positive control signal  $v_e$ ) where the PWM signal is compressed and vice versa. This is observed by looking at the control signal  $v_e$  in Fig. 9.15.

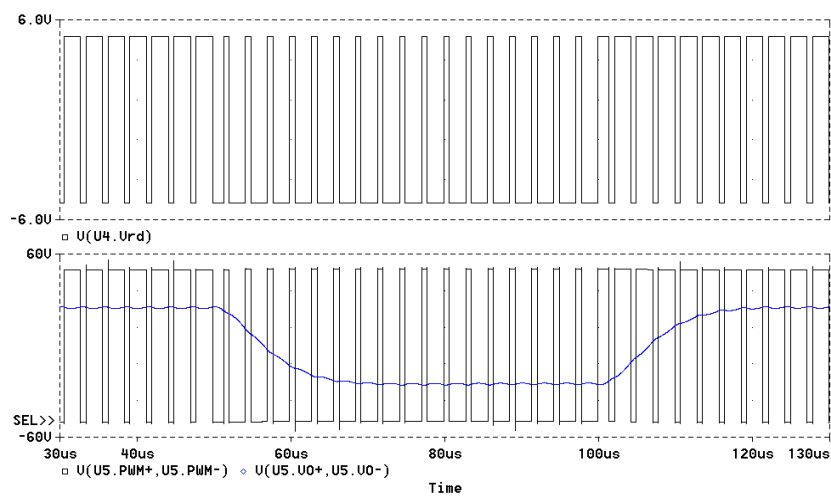


Fig. 9.16 A simulation of the excellent transient response characteristics of PEDEC VFC1. Close investigation of the pulse output  $v_p$  shows exact and *instant* amplification of the reference. The explanation is that PEDEC VFC1 only “works” when errors are generated, and does not affect the amplification otherwise.

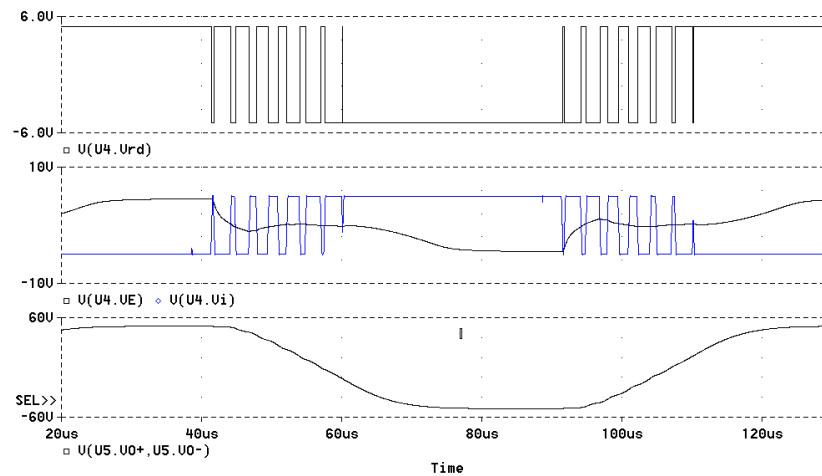


Fig. 9.17 A simulation of a severe 50% overload situation for PEDEC VFC1. Top – Clipping reference. Mid – Control signal to the PEDEC unit and integrated reference. Bottom- The resulting output with 50% overload. The recovery from overload is instant, and the clipping characteristics are as acceptable.

#### *Stability and overload*

An interesting characteristic of PEDEC control is that PEDEC will not oscillate in the traditional way at some unity gain frequency above the audio band, since the correction range is limited. Accordingly, the stability is limited and the effects thereof are equally limited (no tweeter burn out etc.). Another interesting aspect is the excellent transient response of the control system. This instant transient response is illustrated in Fig. 9.16.

The special characteristics in overload situations are simulated in Fig. 9.17. The clipping characteristics and recovery from overload very satisfying. Correspondingly, the minimum pulse width constraint merely indicates the range where the correction afforded by PEDEC VFC will correspond to theory.

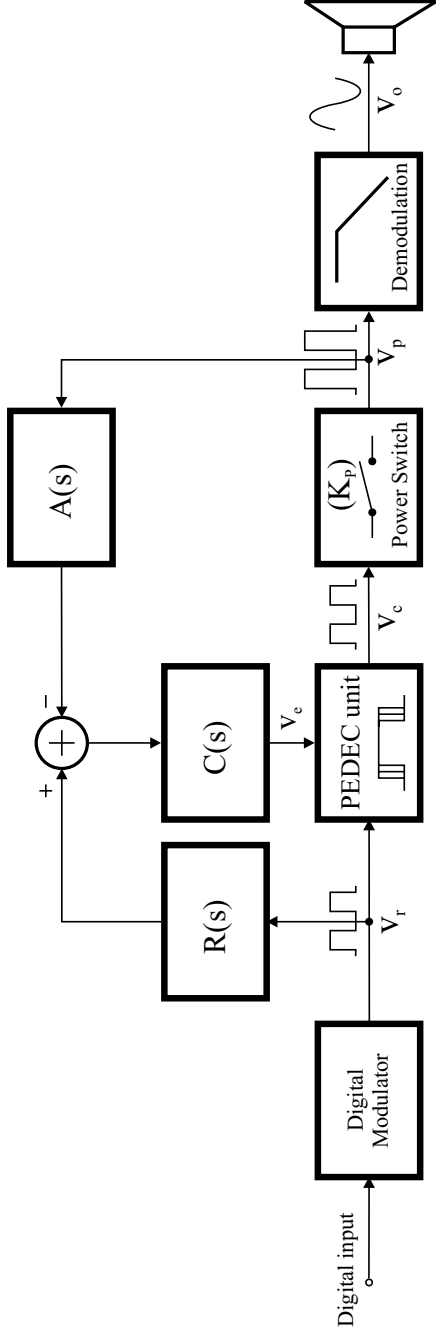


Fig. 9.18 PEDEC VFC2 Topology.

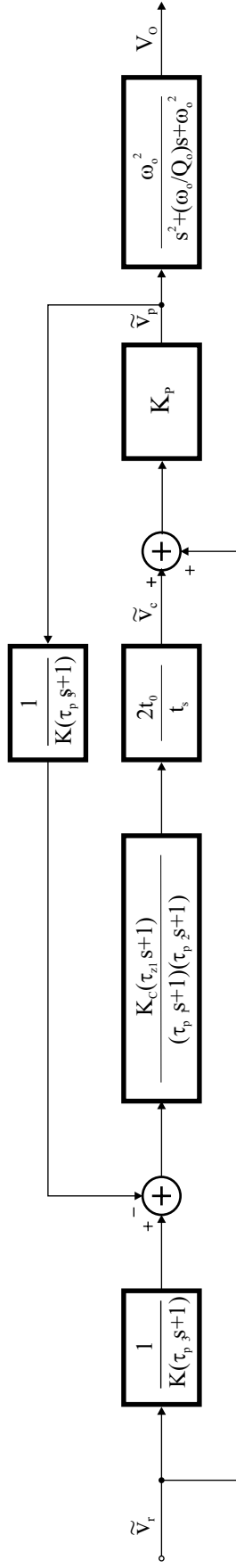


Fig. 9.19 Linear model of PEDEC VFC2 topology with all compensator elements defined. PEDEC VFC2 is characterized by first order error estimation.

## 9.5 PEDEC VFC2

Fig. 9.18 shows the general block diagram for PEDEC VFC2. The topology is closely related to VFC1, in that the feedback source is the switching power stage output. The significant difference lies in the error estimation, which is based on first order reference shaping in that the reference shaping block and feedback path compensator now have first order characteristics. The motivation of this modified error estimation is a simplification of the feedback block (in terms of bandwidth requirement). Recall that pulse modulated signals are inherently *analog*, so there are no essential advantages in maintaining the signals “digital” or pulse modulated at the difference point where reference and attenuated output are compared. On the contrary, it is of primary importance to optimize the estimation of *relevant* errors, i.e. the errors that are introduced in terms of distortion and noise within the audio band. Appropriate first order filtering on the pulse-modulated signal does not change this error estimation within the target frequency band.

### 9.5.1 Analysis

Fig. 9.19 shows the complete linear system model for the proposed PEDEC VFC2 controller. The individual components that constitute the topology are:

$$\begin{cases} C(s) = K_C \frac{(\tau_{z1}s + 1)}{(\tau_{p1}s + 1)(\tau_{p2}s + 1)} \\ A(s) = K_P k_{PEDEC} \\ B(s) = \frac{1}{K} \frac{1}{\tau_{p3}s + 1} \\ R(s) = \frac{1}{\tau_{p3}s + 1} \end{cases} \quad (9.21)$$

Again, the proposed compensator  $C(s)$  is a tradeoff compromise between loop shaping freedom and complexity. The reference shaper and feedback path compensator poles are matched for optimal error estimation. From

Fig. 9.19, the resulting loop transfer is derived:

$$L(s) = \frac{K_C K_P k_{PEDEC}}{K} \frac{(\tau_{z1}s + 1)}{(\tau_{p1}s + 1)(\tau_{p2}s + 1)(\tau_{p3}s + 1)} \quad (9.22)$$

The resulting loop transfer function is identical to VFC1. The resulting transfer function of the system is equally devised from the linear model in

Fig. 9.19:

$$\begin{aligned} H(s) &= R(s) \underbrace{\frac{C(s)A(s)}{1 + A(s)B(s)C(s)}}_{H_A} + \underbrace{\frac{K_P}{1 + A(s)B(s)C(s)}}_{H_B} \\ &= \frac{K_P [R(s)C(s)A(s) + 1]}{1 + A(s)B(s)C(s)} \end{aligned} \quad (9.23)$$

The expression differs mainly from (9.17) in that the reference shaper influences  $H_A(s)$ .

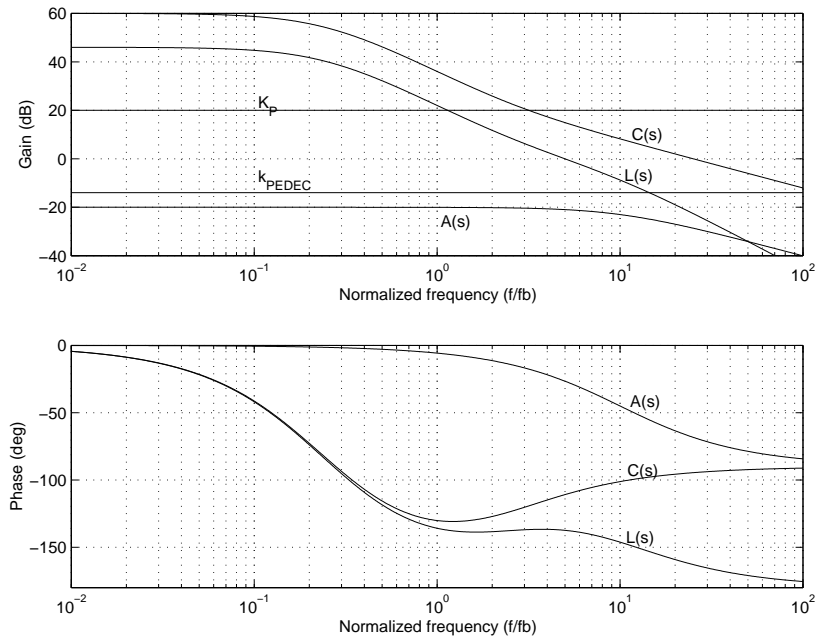


Fig. 9.20 Loop components and resulting loop transfer function of PEDEC VFC2 case example.

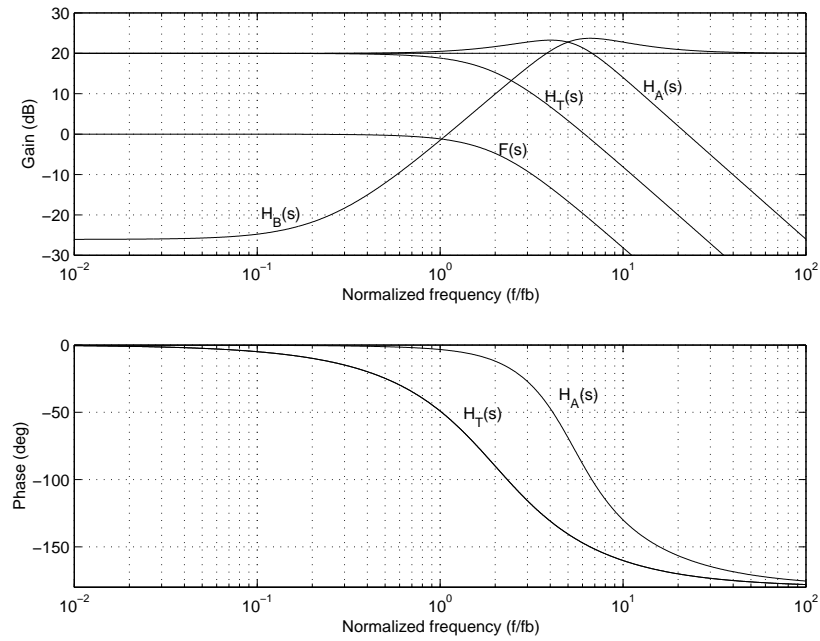


Fig. 9.21 Contributions to total system response for PEDEC VFC2

Assuming, that the pole  $s = \tau_{p3}^{-1}$  is placed at a frequency well beyond the unity gain frequency of the control loop, the closed loop approximation will be as for VFC1:

$$H(s) \approx \begin{cases} K & (f < f_u) \\ K_P & (f \gg f_u) \end{cases} \quad (9.24)$$

And  $H_T(s) = H(s)F(s)$ .

### 9.5.2 PEDEC VFC2 loop shaping

Despite the topological differences, the PEDEC VFC1 parameters also provide pleasant characteristics for PEDEC VFC2 topology. Since the loop transfer functions are identical, PEDEC VFC1 will be identical to PEDEC VFC2 in terms of performance and robustness.

### 9.5.3 Case example

A case example is considered with the same fundamental parameters as PEDEC VFC1. The results will only be discussed briefly, with focus on the differences to PEDEC VFC1.

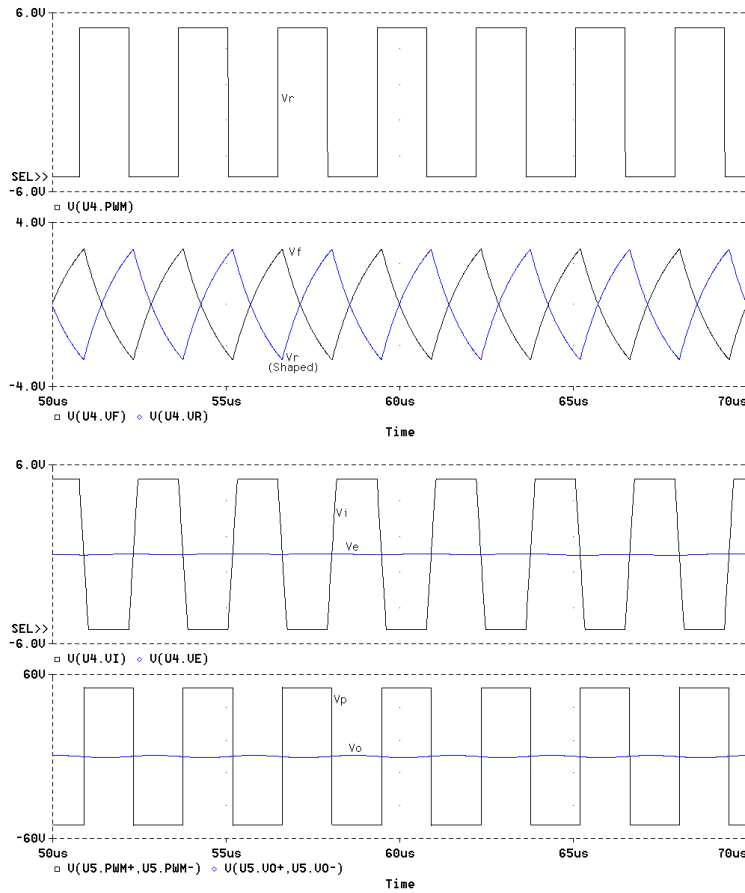


Fig. 9.22 Essential signals in the PEDEC VFC2 controlled system. From top to bottom - Pulse modulated reference, shaped reference and feedback  $v_f$ , PEDEC unit signals  $v_e$ ,  $v_i$  and finally the resulting corrected power stage output.

Fig. 9.20 shows the resulting characteristics of the loop. Fig. 9.21 shows the resulting closed loop transfer functions. The reference shaping does not influence the transfer characteristics notably, since the pole is placed considerably above the loop bandwidth where the direct feed through path  $H_{B,CL}(s)$  dominates the system characteristics.

The results of functional simulation of the system are shown in Fig. 9.22. Observe, how the reference and feedback path compensator are significantly different from PEDEC VFC1, as a consequence of the first order filtered error estimation. Note, how the error signal to the PEDEC unit is nearly free from HF components. VFC2 has been investigated on the same points as PEDEC VFC1 in terms of error correction, robustness and stability. The results are exactly as for VFC1, and the first order filtered error estimation does as such not compromise performance. As shown with the practical evaluation in Chapter 10, performance can be gained due to simpler controller implementation. To conclude, the investigations of the modified PEDEC VFC2 topology has shown that the error estimation may well be based on modified reference. In terms of compensator implementation, PEDEC VFC2 is clearly preferable compared to PEDEC VFC1.

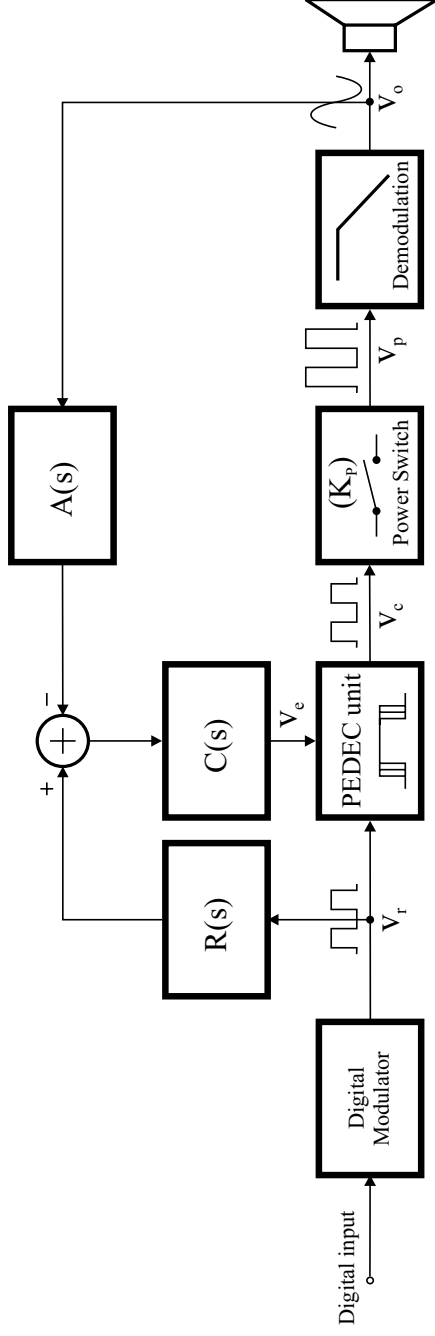


Fig. 9.23 PEDEC VFC3 Topology.

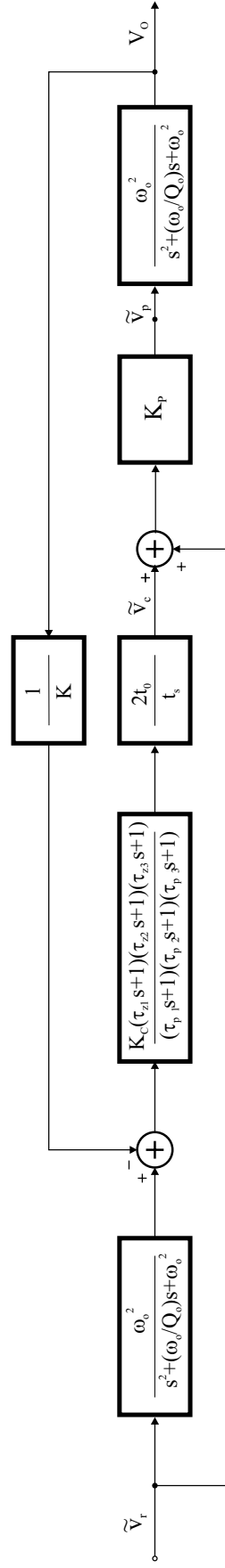


Fig. 9.24 Linear model of PEDEC VFC3 Topology with all compensator elements defined. The topology is characterized by global feedback and error estimation based on second order reference shaping.

## 9.6 PEDEC VFC3

Recall that PEDEC can be considered as a general control method for improved power amplification of a pulse-modulated signal. The generality of the principle means that it can be used advantageously in combination with a range of different control structures. To illustrate this generality, a global feedback topology, defined as PEDEC VFC3, will be investigated. A block diagram for the topology is shown in Fig. 9.23. For optimal error estimation, the reference should resemble the A-block best possible i.e. the R-compensator should match the second order demodulation filter, leading to second order reference shaping.

### 9.6.1 Analysis

The linear model for PEDEC VFC3 is shown in Fig. 9.24. The components of the controller are:

$$\left\{ \begin{array}{l} C(s) = K_C \frac{(\tau_{z1}s+1)(\tau_{z2}s+1)(\tau_{z3}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)} \\ A(s) = K_P k_{PEDEC} \\ B(s) = \frac{1}{K} \\ R(s) = \frac{\omega_o^2}{s^2 + \frac{\omega_o}{Q_o}s + \omega_o^2} \end{array} \right. \quad (9.25)$$

This leads to the following loop transfer function  $L(s)$ :

$$L(s) = \frac{k_{PEDEC} K_C}{K_P} \frac{(\tau_{z1}s+1)(\tau_{z2}s+1)(\tau_{z3}s+1)}{(\tau_{p1}s+1)(\tau_{p2}s+1)(\tau_{p3}s+1)} \frac{\omega_o^2}{s^2 + \frac{\omega_o}{Q_o}s + \omega_o^2} \quad (9.26)$$

The system transfer function is equally found from the linear model:

$$\begin{aligned} H(s) &= R(s) \underbrace{\frac{C(s)A(s)F(s)}{1 + A(s)B(s)C(s)F(s)}}_{H_A} + \underbrace{\frac{K_P F(s)}{1 + A(s)B(s)C(s)F(s)}}_{H_B} \\ &= \frac{F(s)K_P [R(s)C(s)A(s) + 1]}{1 + A(s)B(s)C(s)} \end{aligned} \quad (9.27)$$

### 9.6.2 PEDEC VFC3 Loop shaping

Except for the PEDEC unit, the loop is equivalent to the proposed linear VFC1 in Chapter 6. Subsequently, the loop shaping approach can be transformed directly to PEDEC VFC3. The parameters are given in Table 9.3. The stability and robustness will be as the VFC1 in Chapter 6, under the assumption that PEDEC operates within the correction range.

Parameter	Value	Comment
$k_{PEDEC} = \frac{2t_o}{t_s}$	$\frac{1}{5}$	Equivalent PEDEC unit gain.
$f_{p1} = \frac{1}{\tau_{p1}}$	$\frac{1}{20} f_u$	Loop parameter
$f_{p2} = \frac{1}{\tau_{p2}}$	$\frac{1}{20} f_u$	Loop parameter
$f_{p3} = \frac{1}{\tau_{p3}}$	$3f_u$	Loop parameter
$f_{z3} = \frac{1}{\tau_{z3}}$	$\frac{1}{3} f_u$	Loop parameter
$f_{z1} = f_{z2}$	$f_o$	Compensation of output filter
$f_o$	2	Demodulation filter / reference shaping filter
$Q_0$	$\frac{1}{\sqrt{3}}$	Q of reference and demodulation filter

Table 9.3 Proposed parameters for PEDEC VFC3.

### 9.6.3 Case example

The case example considered has  $f_u = 5$ . Fig. 9.25 shows the system the loop components and the resulting loop transfer function and Fig. 9.26 shows the response of the closed system. PEDEC VFC3 suffers from the requirement for a high compensator gain at high frequencies, which requires a wide-band controller.

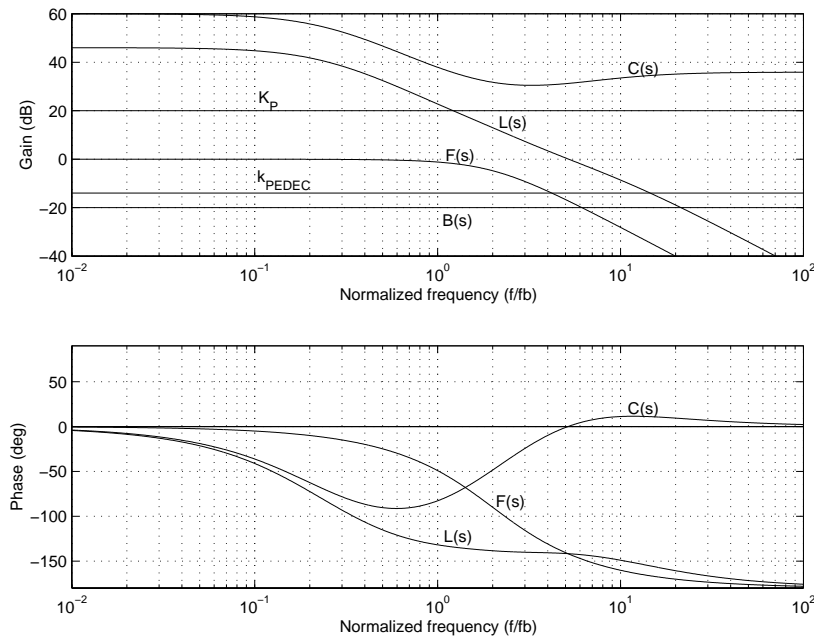


Fig. 9.25 Components for PEDEC VFC3 case example and loop transfer function  $L(s)$ .

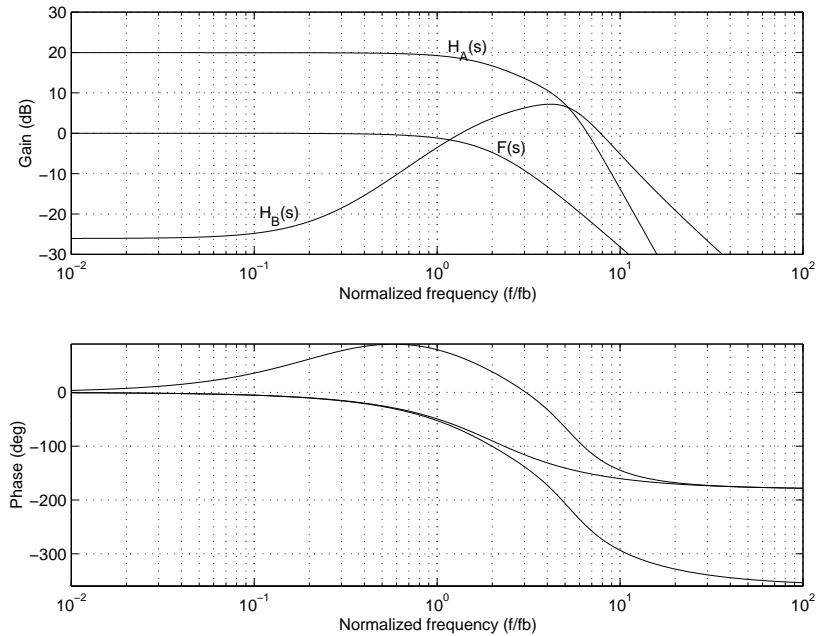


Fig. 9.26 Components of the system and the resulting system transfer function.

### Non-linear simulation

Fig. 9.27 shows a simulation of the essential signals in the PEDEC controller in the idle situation. The simulation shows that the controller is stable and works as desired. Note how the feedback signal  $v_f$  and the reference at the summation point have the opposite phase of the reference signal  $v_r$  at the summation point. A benefit of the second order reference shaping is, that the error control signal to the PEDEC unit has minimal HF-content. PEDEC VFC3 has been simulated using the same simulation sessions as for the other topologies. The controller works exactly as desired but there are special considerations and pitfalls when using this topology. A special consideration is, that the reference shaper should match the demodulation filter reasonably; in order to minimize the correction space needed to compensate for such a mismatch. The general error correction capability corresponds has been found to correspond with theory. Fig. 9.28 shows the simulation of PTE error correction.

## 9.7 Extensions

Due to the minimal pulse width constraint, three-level (BD) PWM schemes are not directly applicable in combination with PEDEC. Some changes in the basic system topology is needed, i.e. a PEDEC controller is needed for each of the modulators driving the two half-bridges. An area of future research is to develop PEDEC controllers for alternative modulation methods as three level systems. Furthermore, only three simple control methods have been presented in this chapter to illustrate the general characteristics of PEDEC. Other control systems may be investigated if the correction offered by the three proposed topologies is not sufficient. Finally, the issue of PEDEC unit realization is a field of its own. Other control functions may be investigated, e.g. non-linear control functions. Furthermore, alternative realizations of the linear control function are an area of future research, although the non-linear simulations suggest that the approach is very feasible.

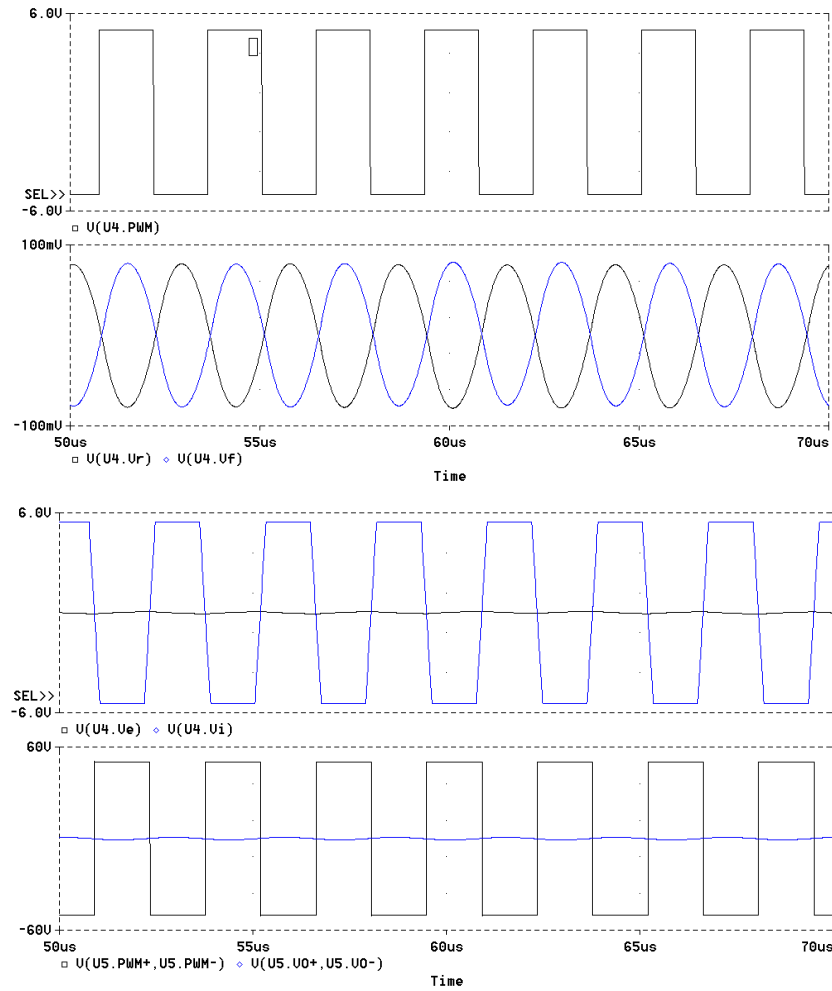


Fig. 9.27 Functional simulation of PEDEC VFC3. From top to bottom – Pulse modulated input, feedback  $v_f$  and shaped reference  $v_r$ , then  $v_i$  and the error signal  $v_e$  and finally the compensated power stage output signals.

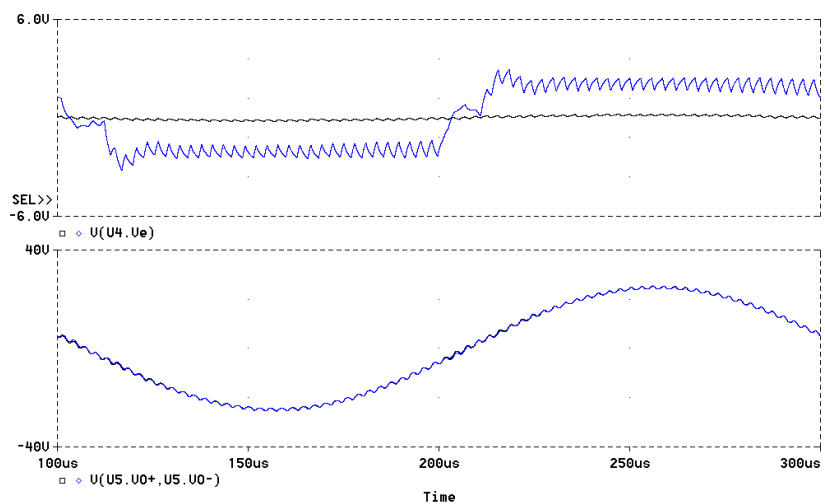


Fig. 9.28 Simulation of PEDEC VFC3 system with  $t_D=0ns$  and  $t_D=100ns$ .  $f=5KHz$ .  $M=0.5$ . Both the linear gain error and distortion are reduced (bottom= $v_o$ ). The controller reduces THD by 25dB. The anti-distorting PEDEC unit input  $v_e$  (top) clearly shows the nature of the distortion.

## 9.8 Summary

This chapter has been devoted to the complicated issue of error correction in systems without an analog LF reference. A novel pulse referenced error correction principle – Pulse Edge Delay Error Correction (PEDEC) – has been proposed. The method uses a pulse-modulated signal as reference for error correction, and performs a re-timing of the pulses edges to compensate for power stage and filter errors. PEDEC was first introduced as a general method for enhanced power amplification of a pulse modulated signal. The desired linear control function was defined and a method of realizing this control function by a PEDEC unit was presented.

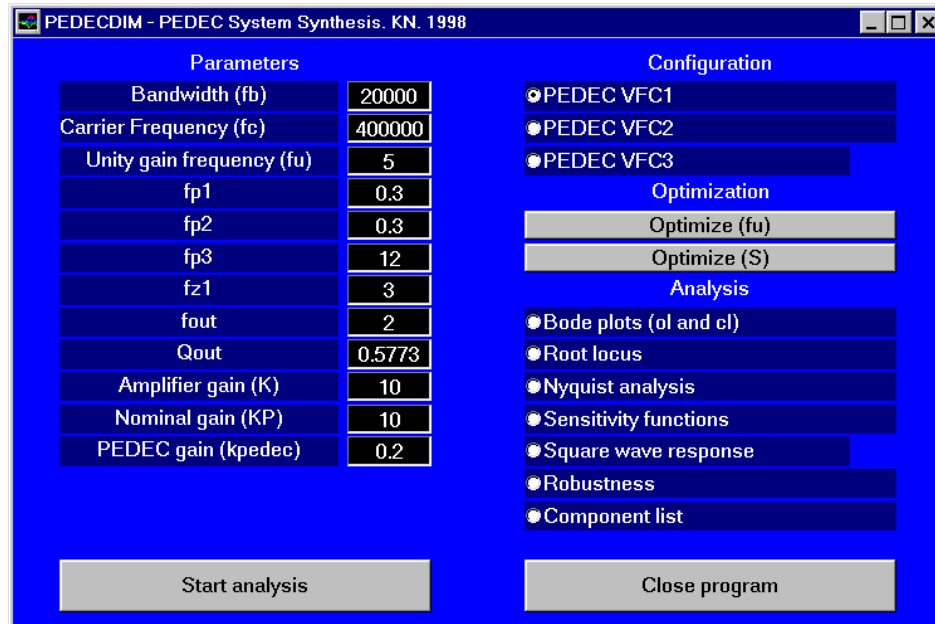
Three simple PEDEC based PMA topologies were proposed with different characteristics in terms of error estimation and feedback source. Loop shaping was addressed, and illustrated by example for the three digital PMA topologies. All topologies proved to realize a significantly reduced sensitivity to any error source existing in a switching power amplification stage. It is concluded, that PEDEC has several interesting properties, some of which are somewhat different from other error correction systems. Three important properties are outlined below:

- *Simplicity.* The proposed system is build of simple linear active components and by resistors and capacitors, causing only a marginal increase in complexity and cost compared to a non-controlled system.
- *Performance.* PEDEC controller can correct all error types and equally important - the improvements are easily *controlled* with the system model.
- *General pulse referenced control scheme.* The inherent pulse referenced nature of the control system leads to an interesting independence of modulation method.

Based on the detailed investigation in both time and frequency domain of the principle, PEDEC is concluded to be a simple and efficient approach to power stage error correction, which makes the realization of high quality digital PMA systems more practical.

### 9.8.1 PEDECDIM - GUI based PEDEC design toolbox for MATLAB

A GUI controlled MATLAB toolbox for systematic, automated and consistent design of PEDEC based digital PMAs has been developed. The graphical user interface is shown below:



Clearly, the interface has some similarity with LCONDIM and MECCDIM, and PEDECDIM fundamentally has the same functionality. Based on the primary amplifier input parameter specifications the interface gives access:

- PEDEC control system synthesis and verifications.
- Controller component synthesis for low-level non-linear simulation.
- Manual access to individual parameters for individual fine-tuning